What is claimed is:

1. A traffic concentrator for combining a plurality of digital data streams into at least one higher speed digital data stream, the traffic concentrator comprising:

a plurality of inputs adapted to receive the plurality of digital data streams;

a memory having first and second portions;

a control circuit, coupled to the plurality of inputs and the memory, the control circuit generating control signals for storing data from the plurality of digital data streams in one of the first and second portions of the memory during a first time slot for retrieval from the portion of the memory during a subsequent time slot for combination and transmission as the at least one higher speed digital data stream.

2. The traffic concentrator of claim 1, wherein the memory comprises a dual port, random access memory.

3. The traffic concentrator of claim 2, wherein the memory comprises a number of columns equal to the number of the plurality of digital data streams and a number of rows equal to twice the number of bits per time slot.

4. The traffic concentrator of claim 1, wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways.

5. A method for bundling a plurality of digital data streams with a first speed to at least one digital data stream with a second, higher speed, the method comprising:

during even time slots in the plurality of digital data streams:

storing data from the plurality of digital data streams in a first memory portion, and

reading data from a second memory portion for transmission on the at

least one digital data stream with a second, higher speed; and

during odd time slots:

storing data from the plurality of digital data streams in the second memory portion, and

reading data from the first memory portion for transmission over the at least one digital data stream with a second, higher speed.

6. The method of claim 5, wherein storing data from the plurality of digital data streams in a first memory portion comprises storing data from a plurality of pulse code modulated (PCM) highways.

7. The method of claim 5, wherein storing data from the plurality of digital data streams in a first memory portion comprises:

associating each column of the first memory portion with a selected one of the plurality of digital data streams;

storing the first bit of each of the plurality of digital data streams in a first row of the first memory portion, each bit stored in the column associated with its digital data stream; and

storing subsequent bits of each of the plurality of digital data streams in subsequent rows of the first memory portion, each bit stored in the column associated with its digital data stream.

8. The method of claim 5, wherein reading data from a second memory portion for transmission on the at least one digital data stream with a second, higher speed comprises reading the data from the second memory portion one time for each of the at least one digital data stream with a second, higher speed.

9. The method of claim 5, wherein reading data from a second memory portion for

transmission on the at least one digital data stream with a second, higher speed comprises:

reading the data from the second memory portion one time for each of the at least one digital data stream with a second, higher speed; and

for each reading of the data from the memory, forming at least one digital data stream with a second, higher speed from a portion of the stored data from the plurality of digital data streams.

10. A de-concentrator for de-bundling a first plurality of digital data streams with a first speed into a second plurality of lower speed digital data streams, the de-concentrator comprising:

a plurality of inputs, each adapted to receive data over one of the first plurality of digital data streams;

a plurality of memory devices, each divided into a first portion and a second portion; and

a control circuit, coupled to the plurality of inputs and the plurality of memory devices, wherein data from a portion of a time slot of the first plurality of digital data streams is selectively stored in one of the first and second portions of each of the plurality of memory devices while data from another time slot of the first plurality of digital data streams is read from the other of the first and second portions of the plurality of memory devices to provide the second plurality of lower speed digital data streams.

11. The de-concentrator of claim 10, wherein the plurality of memory devices comprises a plurality of dual port memory devices.

12. The de-concentrator of claim 10, wherein the control circuit stores interleaved data for lower speed digital data streams in rows of the plurality of memory devices.

13. The de-concentrator of claim 10, wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams.

14. The de-concentrator of claim 10, wherein the first plurality of digital data streams comprises five 8 MHz pulse code modulation (PCM) highways and the second plurality of lower speed digital data streams comprises twenty 2 MHz PCM highways.

15. A method for de-bundling a first plurality of digital data streams from a second plurality of higher speed digital data streams, the method comprising:

receiving a first time slot of the second plurality of higher speed digital data streams;

sequentially storing selected portions of the first time slot of the second plurality of higher speed digital data streams in a first portion of a plurality of memory devices; and

simultaneously reading the data out of the first portion of each of the plurality of memory devices to provide the first plurality of digital data streams during a subsequent time slot of the second plurality of higher speed digital data streams.

16. The method of claim 15, wherein receiving a first time slot of the second plurality of higher digital data streams comprises receiving five 8 MHz digital data streams.

17. The method of claim 15, wherein sequentially storing selected portions comprises storing one-quarter of a time slot of data in each of the plurality of memory devices.

18. The method of claim 15, and further comprising sequentially enabling the plurality of memory devices to store data during a time slot of the second plurality of higher speed digital data streams.

19. A method for de-bundling a first plurality of digital data streams from a second plurality of higher speed digital data streams, the method comprising:

receiving a first time slot of the second plurality of higher speed digital data streams;

sequentially enabling a plurality of memory devices to store data during each time slot of the second plurality of higher speed digital data streams;

storing selected portions of the first time slot of the second plurality of higher speed digital data streams in a first portion of a plurality of memory devices when enabled; and

simultaneously reading the data out of the first portion of each of the plurality of memory devices to provide the first plurality of digital data streams while data is stored in a second portion of the plurality of memory devices during a subsequent time slot of the second plurality of higher speed digital data streams.

20. The method of claim 19, wherein receiving a first time slot of the second plurality of higher digital data streams comprises receiving five 8 MHz digital data streams.

21. The method of claim 19, wherein sequentially storing selected portions comprises storing one-quarter of a time slot of data in each of the plurality of memory devices.

22. A traffic concentrator for combining a plurality of pulse code modulated (PCM) highways into at least one higher speed PCM highway, the traffic concentrator

comprising:

a plurality of inputs adapted to receive the plurality of PCM highways;

a dual port memory having first and second portions;

a control circuit, coupled to the plurality of inputs and the memory, the control circuit generating control signals for storing data from the plurality PCM highways in one of the first and second portions of the memory during a first time slot for retrieval from the portion of the memory during a subsequent time slot for combination and transmission as the at least one higher speed PCM highway.

23. The traffic concentrator of claim 22, wherein the memory comprises a number of columns equal to the number of the plurality of PCM highways and a number of rows equal to twice the number of bits per time slot.

24. The traffic concentrator of claim 22, wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways.